USB Keyboard and Mouse to UART Communication Control Chip CH9350L

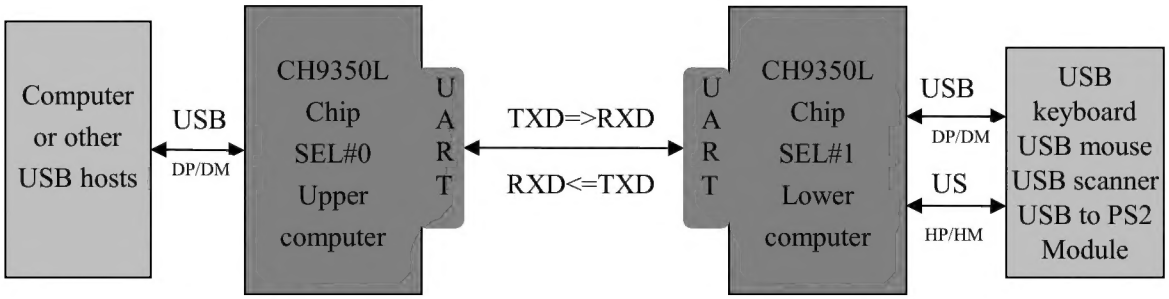
Datasheet

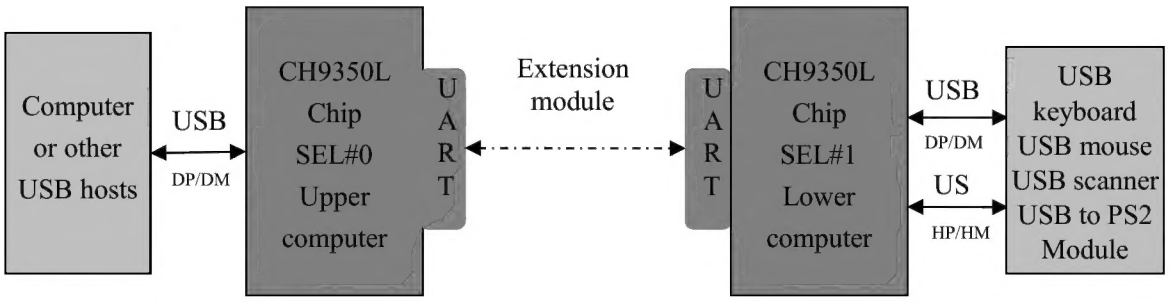
Version: V2.3

http://wch.cn

1. Overview

CH9350L is a USB keyboard and mouse to UART communication control chip. Combined with the simple and easy-to-use features of UART, the USB communication method between USB keyboard/mouse and USB host can be extended to UART, which is convenient for data integration with audio, video and other signals, or can be directly extended through 485 signal 2-wire, which is mainly used for KVM extension, KVM switching, KM synchronization and other applications. The general application diagram for CH9350 is shown below:





Application reference:

1、It is applied to KVM extension and mostly uses working state 1, which supports more HID device types, multimedia functions, HID remote sensing devices, etc.;

2、It is applied to KVM extension + switch, or matrix switch (multiple pairs of keyboard and mouse are used on multiple hosts), and mostly uses working state 2. This state supports multiple pairs of keyboard and mouse corresponding to multiple hosts;

3、It is applied to mouse switch between different screens, synchronization and other functions, and mostly uses working state 3. This state can analyze UART data to know the current position of the mouse and detect whether the cursor is at the edge of the screen, so as to realize the mouse switching function between different screens;

4、It is applied to mouse switch between different screens, synchronization and other functions, and some hosts have extended screens. It mostly uses working state 4, which supports the mouse switching function between different extended screens;

5、It is used independently and mostly used to convert USB keyboard, mouse, scanner and other equipment into serial data application, which can reduce development time and does not need to deal

with USB protocol. It mostly uses state 0 or state 2 of lower computer mode;

6、 Other special applications can be customized and developed.

See Chapter 7 for details.

2. Features

- Support 12Mbps full-speed USB transmission and 1.5MBps low-speed USB transmission, compatible with USB V2.0.
- The USB port of upper computer conforms to the standard HID protocol, and does not need to install additional drivers. It supports Windows, Linux, MAC and other operating systems with built-in HID device drivers.
- One chip can be configured as upper computer mode and lower computer mode, connecting USB-Host and USB keyboard and mouse respectively.
- One mode can be configured to different working states for many applications.
- Support the use of USB keyboard and mouse in the BIOS interface, and support multimedia function keys and USB mouse of different resolutions.
- Support various brands of USB keyboard and mouse, USB wireless keyboard and mouse, USB to PS2 cable, USB scanner, etc.
- The upper computer and the lower computer support hot swap.
- Provide sending status pin, and support 485 communication.
- UART supports 300000/115200/57600/38400 serial communication baud rates.
- Provide built-in crystal oscillator and power-on reset circuit, with simple peripheral circuit.
- Support 5V and 3.3V power supply voltage.
- Provide LQFP-48 lead-free package, compatible with RoHS.

3. Version Change

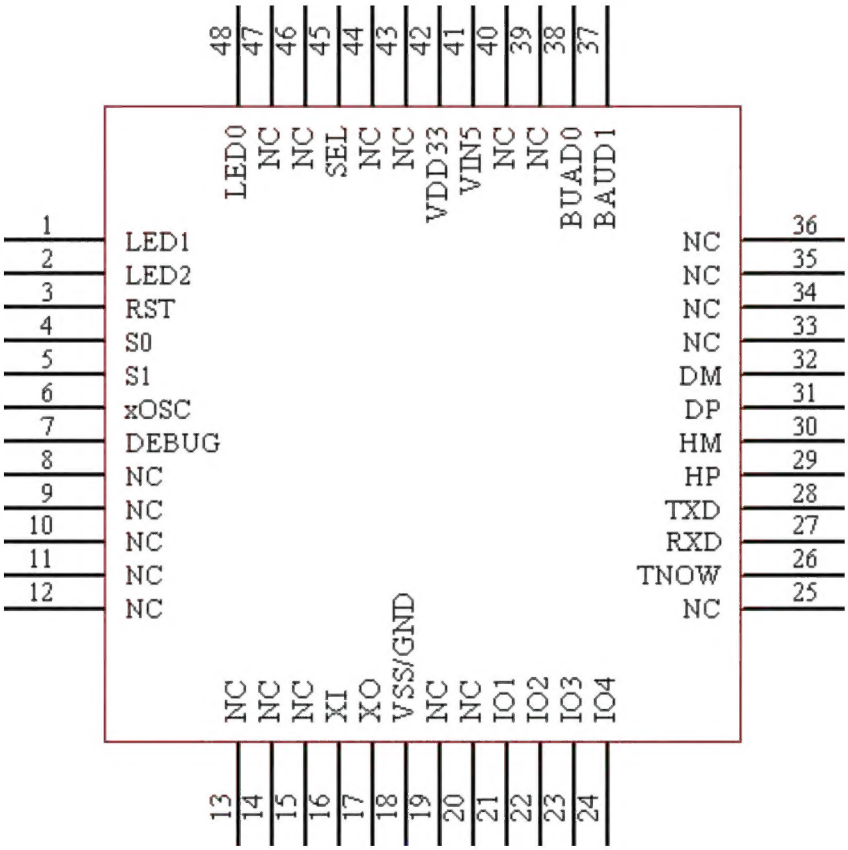
Differences between version V1 and V2: When a single CH9350L (upper computer mode) is connected to PC, there is no USB device in version V1, while there may be a USB keyboard and mouse composite device in version V2; V2 versions are compatible with each other, as shown in Table 3-1 below:

Version	Date	Description
V1.0	June 5, 2015	1、 First release 2、 Mainly applied to 485 mode 2-wire KM extension
V2.1	January 12, 2017	1、 Cannot be mixed with version V10 2、 Support for one-to-many use, as well as the extension of KM switching, used in a variety of KM extension environments 3、 Add remote wake-up function, which can remotely wake up the host through the keyboard and mouse 4、 Add 2 groups of remote IO synchronization status function, which can be used to realize functions such as remote switch 5、 Add various working states and support for more applications, see Chapter 7 for details
V2.2	September 19, 2017	1、 Compatible with version V21 2、 Support set the keyboard indicator status in state 2 3、 Add analog absolute mouse device, state 3 4、 Add support for HID devices such as remote sensing 5、 Support VID/PID modification at the device end, see Chapter 7 for details

V2.3	May 9, 2018	1、 Compatible with version V22 2、 Support one-way communication in state 2/3/4 3、 Add support for a single keyboard or mouse device with a built-in hub 4、 Add state 4 and support for Windows7 and above extension screen switching, see chapter 7 for details

Table 3-1

4. Package



Package	Width of Plastic		Pitch of Pin		Instruction of Package	Ordering Information
LQFP-48	7*7mm		0.5mm	19.7mil	LQFP48-pin patch	CH9350L

5. Pin

Pin No.	Pin Name	Pin Type	Pin Description
48	LED0	Output	Status indication pin
1	LED1	Output	Connection communication indication pin corresponding to port 1 device (DP/DM)
2	LED2	Output	Connection communication indication pin corresponding to port 2 device (HP/HM)
3	RST	Input	External reset input, active at high level

4	S0	Input	Working status configuration pin	S1|S0 11: State 0/1 (default) 10: State 2 01: State 3 00: State 4
5	S1	Input		
6	xOSC	Input	External clock enable pin, active at low level	
7	DEBUG	Output	Reserved, suspended (test pin)	
16	XI	-	Reserved, suspended or reserved pad (crystal oscillator input)	
17	XO	-	Reserved, suspended (crystal oscillator reverse output)	
18	VSS/GND	-	Common ground	
26	TNOW	Output	Sending status pin (can be used for 485 direction control)	
27	RXD	Input	UART data input	
28	TXD	Output	UART data output	
29	HP	USB signal pin	USB bus D+ data line	USB host D+/D-(lower computer port 2)
30	HM	USB signal pin	USB bus D- data line	
31	DP	USB signal pin	USB bus D+ data line	USB host D+/D-(lower computer port 1) USB device D+/D-(upper computer)
32	DM	USB signal pin	USB bus D- data line	
37	BAUD1	Input	Baud rate configuration pin 1, default to pull up	BAUD1|BUAD0 11: 115200 (default) 01：57600 10：38400 00：300000
38	BAUD0	Input	Baud rate configuration pin 0, default to pull up	
41	VIN5	-	5V external power input of internal 5V->3.3V voltage regulator, An external 0.1uF power decoupling capacitor is required.	
42	VDD33	-	Internal voltage regulator output and internal 3.3V working power input, When supply voltage is less than 3.6V, connect VIN5 to input the external power supply, An external 3.3uF power decoupling capacitor is required when the supply voltage is greater than 3.6V	
45	SEL	Input	Chip working mode selection pin, default to pull up	1: lower computer mode (default) 0: upper computer mode
21	IO1	Input/output	Status synchronization pin	Upper computer mode state 1 (output) Lower computer mode state 1 (input)
22	IO2	Input/output	Status synchronization pin	
23	IO3	Input/output	Status synchronization pin	Upper computer mode state 1 (input) Lower computer mode state 1 (output)
24	IO4	Input/output	Status synchronization pin	
8, 9, 10, 11, 12, 13, 14, 15, 19, 20,	NC	-	Reserved, must be suspended	

25, 33, 34, 35, 36, 39, 40, 43, 44, 46, 47			

6. Parameters

6.1 Absolute Maximum Value

Critical value or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged.

Name	Parameter description		Min.	Max.	Unit
TA	Ambient temperature during operation	VIN5=5V or VIN5=VDD33=3.3V	-40	85	℃
TS	Ambient temperature during storage		-55	125	℃
VDD33	Internal working supply voltage (VCC33 connects to power, GND to ground)		-0.4	3.6	V
VIN5	External input power supply voltage (VIN5 connects to power, GND to ground)		-0.4	5.6	V

6.2 Electrical Parameters

Test Conditions: TA=25℃, VIN5=5V, Excluding the Pins Connected to the USB Bus.

Name	Parameter description		Min.	Typ.	Max.	Unit
VIN5	External input supply voltage	VDD33 pin only connects to an external capacitor	3.6	5	5.5	V
		VDD33 pin connects to VIN5	3.0	3.3	3.6	V
VIL	Low level input voltage		-0.4		0.8	V
VIH	High level input voltage		2.0		VDD33+0.4	V
VOL	Low level output voltage (4mA draw current)				0.4	V
VOH	High level output voltage (4mA output current)		VCC-0.4			V
Vpot	Voltage threshold of power-on reset		2.2	2.4	2.5	V

7. Application and Description

7.1 Hardware Circuit Design

(1) Chip working voltage

When VCC inputs 5V voltage, VDD33 should connect a capacitor not less than 3.3uF to ground (as shown in Figure 7-1 below). When VCC inputs 3.3V voltage, VDD33 should connect to VIN5 pin.

(2) Reset circuit

The CH9350L chip has a built-in power-on reset circuit. Generally, no external reset is required. It is recommended that this pin should be suspended or grounded. The RST pin is used to input a reset signal externally. When the RST pin is at high level, the effective reset signal width is typically 100ns, and the CH9350L chip is reset.

(3) Clock circuit

CH9350L has a built-in clock, generally does not require external input clock signal. The xOSC pin (PIN6) is the external clock input enable pin, active at low level. When the external input clock is enabled, the 12M clock needs to be input externally.

(4) Communication and status indication

The LED0 pin is a status indication pin, which is at high level by default. If the chip enters the upper computer mode, this pin is at low level, and changes to high level after communicating with the PC. When the PC is not connected, the current working mode can be judged according to this pin. If the chip enters the lower computer mode, after connecting with USB device, the high/low level of the pin changes, indicating that the operation of the device fails, possibly because the device type is not supported. The pin output level is 3.3V.

LED1 and LED2 correspond to the connection communication status indicator of port 1(DP/DM) and port 2(HP/HM) respectively, which are at high level by default. After successfully enumerating the device in the lower computer mode, they are at low level. And after connecting to the host and successful initialization in the upper computer mode, they are at low level. When the keyboard is pressed or the mouse moves, the corresponding LEDx pin will occur high/low level change (hold time of about 260ms) and fix at low level finally. When the pin occurs high/low level, the lower computer indicates that the valid key value data has been obtained for the keyboard or mouse to which the device is connected, while the upper computer indicates that the valid data of the keyboard or mouse has been successfully transmitted to the host. The pin output level is 3.3V.

(5) IO status synchronization

CH9350L consists of four status synchronization IO pins, which are divided into two groups and at high level by default.

IO1/IO2 is input pin in lower computer mode and output status indication pin in upper computer mode. When the pin at the lower computer end is at low level, the corresponding pin at the upper computer end outputs low level. And when the pin at the lower computer end is at high level, the corresponding pin at the upper computer end outputs high level.

IO3/IO4 is input pin in upper computer mode and output status indication pin in lower computer mode. When the pin at the upper computer end is at low level, the corresponding pin at the lower computer end outputs low level. And when the pin at the upper computer end is at high level, the corresponding pin at the lower computer end outputs high level. It is supported when working at state 1.

(6) Working status configuration pin

S0 and S1 pins (PIN4|PIN5) are working status configuration pins and default to input pull-up, that is, default to working at state 0/1. The working state of upper or lower computer mode can be switched to state 2, state 3 and state 4 by the configuration pin, which can be used in more applications. The working state configuration is as shown in Table 7-1:

S0	High	Low	High	Low	Pin level status
S1	High	High	Low	Low	
Working status	State 0/1 (default)	State 2	State 3	State 4	

Table 7-1

(7) Baud rate configuration

BAUD0 and BAUD1 pins (PIN38|PIN37) are baud rate configuration pins and default to input pull-up, that is, the default baud rate is 115200. It is recommended to use the default baud rate. The baud rate can be adjusted to 38400, 57600, 115200 and 300000 by the configuration pins. The corresponding relationship is shown in Table 7-2:

BAUD0	High	High	Low	Low	Pin level status
BAUD1	High	Low	High	Low	
Baud rate	115200 (default)	57600	38400	300000	Unit: bps

Table 7-2

(8) USB interface

Upper computer mode: DP/DM is the D+/D-data line of the USB bus, connecting the USB-Host.

Lower computer mode: DP/DM (port 1) and HP/HM (port 2) are two sets of D+/D-data lines of USB bus, connecting keyboard and mouse devices.

(9) State 2/3/4 support one-way communication

The upper computer works in the state 2/3/4, and the TXD pin is grounded; the lower computer works in the state 2/3/4, and the RXD pin is grounded; then one-way transmission of the corresponding working state can be realized, that is, the data is only transmitted from the lower computer to the upper computer.

(10) Reference circuit

The chip supports 5v and 3.3v working voltages. The voltage of 5V is used in the following reference circuit, which is the simplest circuit commonly used. If other functions need to be configured, such as using external crystal oscillator, configuring working state and baud rate, etc. you can refer to Parts 1-9 of Section 7.1. Unused pins should be suspended.

The chip working mode configuration pin (SEL) is pulled up by default and can be suspended or connected to VDD33 pin with a pull-up resistor. When power-on or reset, if it is detected at high level, it will enter the lower computer mode. J1 is a communication serial port, with output level of 3.3V, and compatible with 5V. The default baud rate is 115200, with 8 data bits, 1 stop bit, no parity check. The sending status pins are used to control half duplex 485. J2 and J3 are USB interfaces that support USB 2.0 full speed or low speed for connecting USB keyboard and mouse devices. It is recommended that C3 and C4 should not be less than 100uF. The reference circuit diagram of the lower computer is shown in Figure 7-1 below. Note: SEL pin input voltage should not be greater than 3.6V.

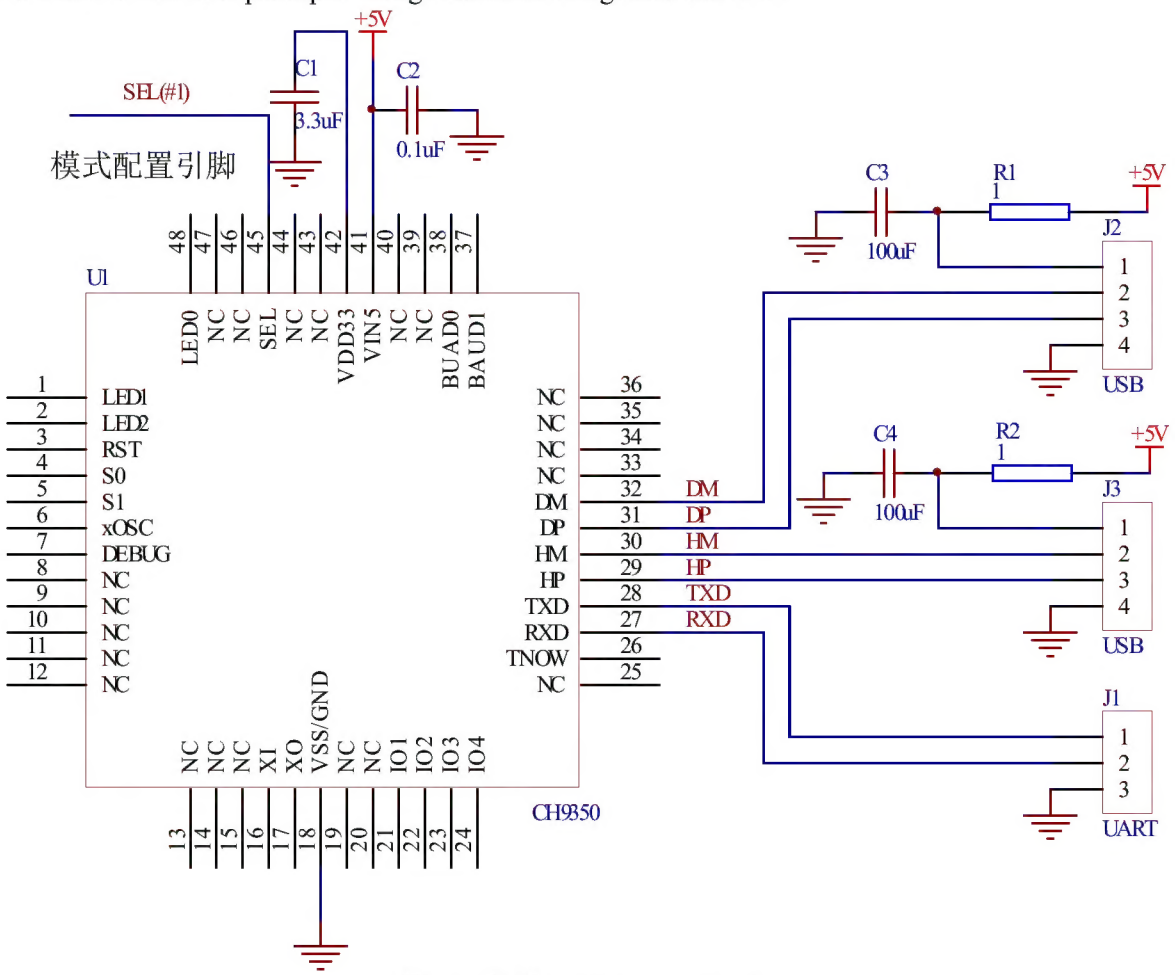


Figure 7-1 Lower computer mode

The chip working mode configuration pin (SEL) is grounded or input low level externally. When power-on or reset, if it is detected at low level, it will enter the upper computer mode. J1 is a communication serial port, with output level of 3.3V, and compatible with 5V. The default baud rate is 115200, with 8 data bits, 1 stop bit, no parity check. The sending status pins are used to control half duplex 485. J2 is the USB interface for connecting computer or other USB hosts. The reference circuit of upper computer is as shown in Figure 7-2 below.

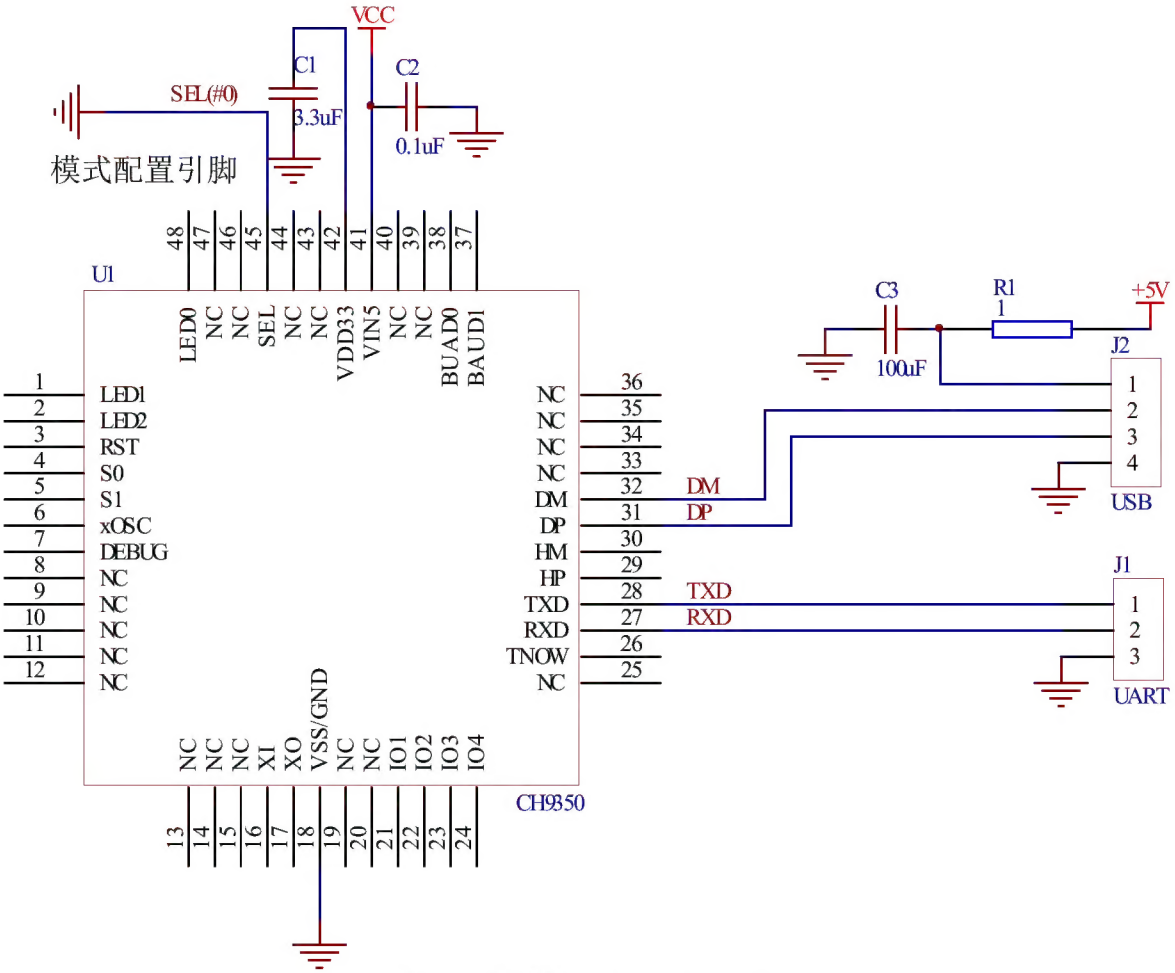


Figure 7-2 Upper computer mode

7.2 Application Reference

1. UART features

The output level is 3.3V and compatible with 5V. The default baud rate is 115200, with 8 data bits, 1 stop bit, no parity check. After the chip enters the upper computer mode, SEL (Pin 45 of the chip) is the UART receiving enable pin in upper computer mode, active at low level (active by default). After the chip enters the lower computer mode, the pin has no other function.

2. Working mode

CH9350L supports 2 working modes, namely the upper computer mode and the lower computer mode. One USB interface (DM-DP) in the upper computer mode for connecting USB-HOST, such as a computer. And two sets of USB interfaces (DM-DP, HM-HP) in the lower computer mode for connecting two USB keyboard and mouse devices.

Different working modes can be selected by configuring SEL pin level state. When chip is powered on or reset, if the SEL pin is detected at high level, it enters the lower computer mode. When the chip is powered on or reset, if the SEL pin is detected at low level, it enters the upper computer mode. 5 different working states are respectively supported in the two modes.

3. Working status

CH9350L supports 5 working states in upper computer mode and lower computer mode respectively. The default state is state 0. When the upper computer mode successfully communicates with lower computer mode, the working state 1, state 2, state 3 or state 4 can be realized by the configuration pin, see description in 7.1.6. The differences among the five working states are as follows:

Upper computer mode

State 0 is the default power-on working state, it simulates the keyboard and mouse composite device;

State 1 indicates that CH9350L is used in pairs, and the simulated device depends on the USB mouse and keyboard HID device connected to the lower computer;

State 2 supports VID/PID modification, it simulates the keyboard and mouse composite device;

State 3 supports VID/PID modification, it simulates the keyboard and mouse composite device and is an absolute displacement mouse;

State 4 supports VID/PID modification, it simulates the keyboard, mouse and HID digitizers composite device and can be used in pairs with state 3 and state 4 of the lower computer.

The VID/PID modification command is as follows:

0x57	0xAB	0x10	2-byte VID (little endian)	2-byte PID (little endian)

Lower computer mode

State 0 is the default power-on working state, it can operate two USB keyboard and mouse HID devices;

State 1 indicates that CH9350L is used in pairs, supporting HID devices such as multimedia and remote sensing;

State 2 only supports standard keyboard and mouse (relative displacement), not multimedia and other HID class devices;

State 3 only supports standard keyboard and mouse, not multimedia and other HID class devices;

State 4 only supports standard keyboard and mouse, not multimedia and other HID class devices.

3.1 State 0

State 0 is the default power-on working state, it will always work in this state when used alone. Some commands need response data, please refer to the communication protocol in Section 7.4 for details. When CH9350L used in pairs communicates successfully, it will enter state 1.

Upper computer: it simulates the keyboard and mouse composite device. For the key value part of the valid key value frame that can be received, please refer to the protocol in state 2. If a status request frame is received in this state, it will send a status response frame.

Lower computer: it can operate the keyboard and mouse device with two USB interfaces. In this state, the status request frame will be sent.

3.2 State 1

When CH9350L is used in pairs, it switches from state 0 to state 1. This mode is mostly used for KM extension.

Upper computer: it simulates the keyboard and mouse HID composite device. The device type depends on the device connected to the lower computer. If a status request frame is received in this state, it will send a status response frame.

Lower computer: it can operate the keyboard and mouse device with two USB interfaces. In this state, the status communication frame, device connection frame, valid key value frame, reset delay command and status change command will be sent.

3.3 State 2

If pin 4 of the chip is at low level and pin 5 is at high level, it will enter this state. It can be used for KM extension, switching, sharing and other functions. Multimedia function keys are not supported in this state.

Upper computer: When receiving a status change command in this state, it will send a status response frame to simulate a keyboard and mouse composite device. The mouse is a relative mouse and the keyboard is a standard keyboard under the BIOS protocol.

Lower computer: In this state, the valid key value frame and status change command will be sent to connect a pair of USB keyboard and mouse devices.

3.4 State 3

If pin 5 of the chip is at low level and pin 4 is at high level, it will enter this state. It can be used for KM extension, switching, sharing and other functions. Multimedia function keys are not supported in this state.

Upper computer: When receiving a status change command in this state, it will send a status response frame and simulate a keyboard and mouse composite device. The mouse is an absolute mouse and the keyboard is a standard keyboard under the BIOS protocol.

Lower computer: In this state, the valid key value frame and status change command will be sent to connect a pair of USB keyboard and mouse devices.

3.5 State 4

If pin 5 of the chip is at low level and pin 4 is at low level, it will enter this state. It can be used for KM extension, switching, synchronization, extended screen and multi-host mouse switch between different screens, etc. In this state, multimedia function keys are not supported, and a few keyboards and mice have compatibility problems.

Upper computer: When receiving a status change command in this state, it will send a status response frame to simulate a keyboard, mouse and HID digitizers composite device. The keyboard is a standard keyboard under the BIOS protocol and HID digitizers are absolute displacement.

Lower computer: In this state, the valid key value frame and status change command will be sent to connect a pair of USB keyboard and mouse devices.

Note: Some systems do not support HID Digitizers devices.

4. Communication Protocol

4.1 Device Connection Frame

State 0/1 supports this command, which is sent by the lower computer, received by the upper computer and has no response.

0x57	0xAB	0x81	1-byte ID	2-byte Payload length	Payload	2-byte ID	1-byte parity check

State 1 in lower computer mode will send the data frame when a device property mismatch is detected. The check value is calculated as a sum, in the range of Payload + 2-byte ID.

4.2 Status Request Frame

State 0/1 supports this command, which is sent by the lower computer, received by the upper computer and has response.

0x57	0xAB	0x82	0xA*

State 0/1 in lower computer mode will send status communication frame at fixed intervals. The initial interval is 66ms, and the interval is 1s after normal operation. The last 1 byte is 0xA*, with the high 4 bits being the fixed value and the low 4 bits being the IO status value.

If used alone, working in state 0, it will respond to a specific data frame to CH9350L and stop sending this command. The 11-byte specific data frame is defined as follows:

0x57	0xAB	0x12	0x00	0x00	0x00	0x00	0xFF	0x80	0x00	0x20

Working in state 1, if a specific data frame is received, it will enter state 0. To restore state 1, the following specific data frame can be sent to CH9350L:

0x57	0xAB	0x12	0x00	0x00	0x00	0x00	0xFF	0xFF	0x00	0x20

4.3 Valid Key Value Frame

It is sent by the lower computer, received by the upper computer and has no response.

The valid key value of state 0/1 is as follows:

Type	Length (Byte)	Description			
Frame head	2	Fixed data: 0x57 0xAB			
Command code	1	The code value used to identify the valid key value frame: 0x83/0x88			
Length	1	Length of subsequent data (ID + key value + serial No. + check)			
Labeling	1	7&6&3	Bit5&4	Bit2&1	Bit0
		Reserved	01: keyboard 10: mouse 11: multimedia 00: other	01：HID 10：BIOS 00: Unknown 11: Reserved	0: Port 1 1: Port 2
Key value	variable	Data uploaded by keyboard or mouse			
Serial No.	1	Data frame serial number			
Check	1	1-byte accumulation sum check (key value + serial number)			

Valid key value frame: The data length is less than 72 bytes. The sending interval between data

frames is related to the attribute of the connected device. When data is forwarded, it is sent according to the actual data frame interval.

Command code: The command code is 0x83 when the lower and upper computer mode work in state 1, and the command code is 0x88 when the lower computer mode works in state 0. It is used alone or for the detection of KM hotkey before establishing communication with CH9350L on upper computer in the application of KM hotkey switch. The data will not be transmitted to the host by the upper computer CH9350L.

Key value: State 0 in lower computer mode is the original data of keyboard and mouse, and state 1 is the data of keyboard and mouse with ID. The key value data that the state 0 in upper computer mode can receive is the same as the key value data in state 2; and state 1 can receive the key value data sent by the state 1 in lower computer mode.

The valid key value of state 2/3/4 is as follows:

Frame Head (2 Bytes)	ID (1 Byte)				Key Value (8/7/4 Bytes)
0x57 0xAB	Bit3-7	bit2	bit1	bit0	8-byte keyboard key value data 7/4-byte mouse key value data
	Reserved	Absolute mouse	Relative mouse	Keyboards	

(1) Bit0 set to 1 indicates that the data frame is keyboard data, which is standard 8-byte USB keyboard data under the BIOS protocol.

(2) Bit1 set to 1 indicates that the data frame is relative mouse data, which is 4-byte data with fixed resolution (8 bit): 1-byte button, 1-byte X-axis offset value, 1-byte Y-axis offset value, and 1-byte wheel. The relative value of X-axis and Y-axis is -127 at the minimum and 127 at the maximum. And the positive and negative represent the direction, the positive value represents positive offset, negative value represents reverse offset, and the value represents the relative offset.

(3) Bit2 set to 1 indicates that the data frame is absolute mouse data, which is 7-byte data with fixed resolution (10 bit): 1-byte ID value (fixed value of 0x01), 1-byte button, 2-byte X-axis coordinate value, 2-byte Y-axis coordinate value, and 1-byte wheel. The absolute value of the X-axis and Y-axis is 0 at the minimum and 0x3FF at the maximum, which represents the current cursor coordinate value, that is, the cursor position.

State 2 is relative mouse data, and states 3 and 4 are absolute mouse data. The details are as follows:

State 2/3/4 keyboard data

0x57	0xAB	0x01	8-byte keyboard data

The 8-byte keyboard data is USB standard keyboard data, and the corresponding key values can be parsed by referring to the "Full keyboard Code Value Table". For example:

57 AB 01 00 00 2C 00 00 00 00 00, indicates that the space key is pressed

57 AB 01 00 00 00 00 00 00 00 00, indicates that the space key is released

State 2 mouse data

0x57	0xAB	0x02	4-byte mouse data

The 4-byte mouse data is defined as follows:

Byte0	Byte1	Byte2	Byte3
Button	X-axis relative displacement value	Y-axis relative displacement value	Wheel

State 3/4 mouse data

0x57	0xAB	0x04	7-byte mouse data

The 7-byte mouse data is defined as follows:

Byte0	Byte1	Byte2-3	Byte4-5	Byte6
ID value	Button	X-axis absolute displacement value	Y-axis absolute displacement value	Wheel

When analyzing mouse data, it can be determined whether the current cursor position is at the edge of the screen based on either the maximum absolute displacement value (0x03FF) or the minimum value (0x0000).

Note: Multimedia function keys are not supported in this state, and a few keyboards and mice have compatibility problems. If you have special needs, you can use working state 1.

4.4 Reset Delay Command

State 1 supports this command, which is sent by the lower computer, received by the upper computer and has no response.

0x57	0xAB	0x84

4.5 Working Status Change Command 1

State 0/1 supports this command, which is sent by the lower computer, received by the upper computer and has no response.

0x57	0xAB	0x85	1-byte status value

The status value is the chip working status code.

0x02: The working status of upper computer will switch to state 2;

0x03: The working status of the upper computer will switch to state 3.

4.6 Device Disconnect Command

State 1 supports this command, which is sent by the lower computer, received by the upper computer and has no response.

0x57	0xAB	0x86

The lower computer will send the command when it detects the device is removed, and the upper computer will reset the chip when it receives the command.

4.7 Obtain Version Number Command

State 0/1/2/3/4 supports this command, which is sent by the lower computer, received by the upper computer and has response.

0x57	0xAB	0x87

The command is sent only once and can have no response.

4.8 Status Change Command

State 2/3/4 supports this command, which is sent by the lower computer, received by the upper computer and has response.

0x57	0xAB	0x80	1-byte status value

The lower 4 bits of the status value are the report ID value, and the higher 4 bits are the IO0/IO1 status value.

4.9 Working Status Switch Command 2

State 2/3/4 of upper computer supports this command and has no response.

0x57	0xAB	0x40	1-byte status value

The status value is the chip working status code, which is used to switch the working status of the upper computer. For example: Under working state 3, you can send this command and specify the state value as 4, then it will switch to working state 4.

4.10 Specific Data Frame

The upper computer response 11-byte data frame is defined as follows:

0x57	0xAB	0x12	PID value of 2-byte port 1		PID value of 2-byte port 2	
			Keyboard report value	Current Status	Status value	Fixed value/version number

The valid range of keyboard report value is 0-7, and the report ID is the status value of keyboard indicator. Their correspondence is as follows:

Bit0	Bit1	Bit2	Bit3-Bit7
0: Num Lock off 1: Num Lock on	0: Caps Lock off 1: Caps Lock on	0: Scroll Lock off 1: Scroll Lock on	Reserved

The status value is defined as follows:

Bit7-4	Bit3-0

1010	bit2/bit3 is the current level status value of IO3/IO4
0000 (Only state 3 and state 4 support)	0001: Clear X-axis coordinate value 0010: Clear Y-axis coordinate value 1111: Configure auto clear mode

In applications of mouse switch between different screens, for state 3 and 4, it is needed to change the current absolute coordinate value of X/Y axis when screen switches. The lower computer can receive the following commands:

Clear X-axis coordinate value: 57 AB 12 00 00 00 00 FF FF 01 20

Clear Y-axis coordinate value: 57 AB 12 00 00 00 00 FF FF 02 20

Configure auto clear mode: 57 AB 12 00 00 00 00 FF FF 0F 20

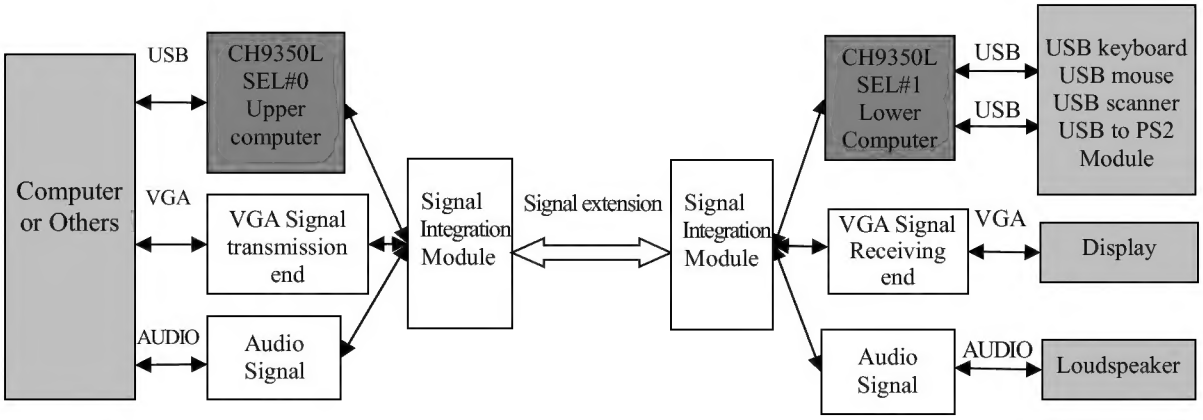
Clear the X-axis coordinate value command, that is, when the mouse moves to the far left or right side of the screen, the current X-axis coordinate value shall be changed when the screen switches at this time, so that the whole process of mouse movement between the two screens is continuous. For example: The current X-axis coordinate value is 0, after switching to another screen, the value shall be changed to the maximum. For Y-axis, it is the same as that of the X-axis. Configure the auto clear mode, and the X-axis and Y-axis coordinate values will cyclically change from 0 to the maximum value. For example: Assuming the current X-axis coordinate value is 0x03FE (the maximum value is 0x3FF), when it moves 5 units next time, the current coordinate value is 0x0003. If the auto clear mode is not configured, when the current coordinate value is the minimum value of 0, the value will not change when moving to the left; if the current coordinate value is the maximum value of 0x03FF, the value will not change when moving to the right.

7.3 Application

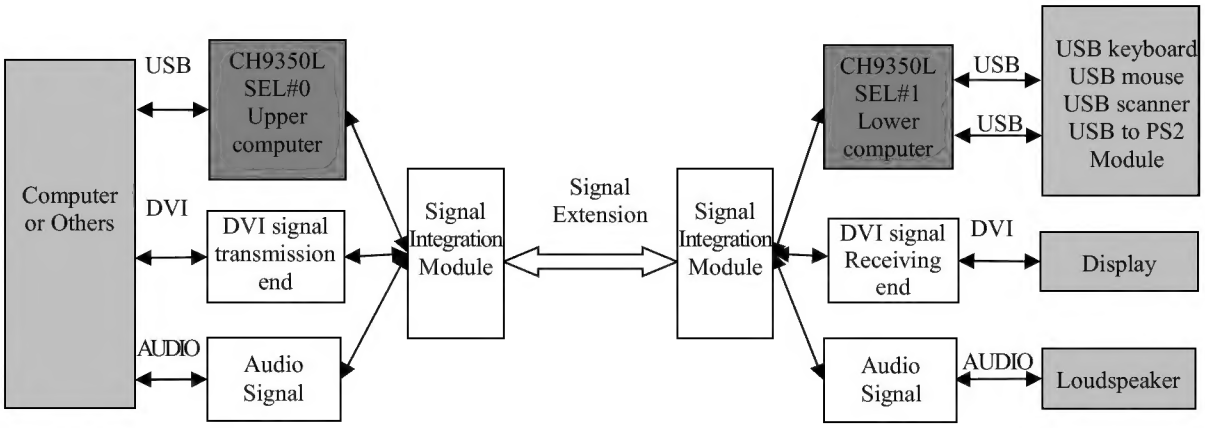
It is applied in industrial control, subway station video, security monitoring, building LED screen, shopping mall advertising, digital signage, visual media teaching, digital KVM, computer remote management and other fields.

7.4 Application Block Diagram

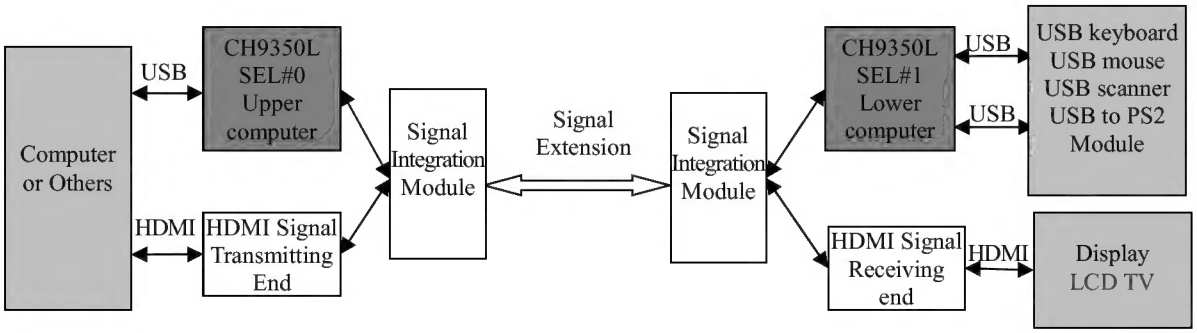
Solution 1: A keyboard, mouse, audio, and video extension solution that integrates USB keyboard and mouse, video signal (VGA signal), and audio signal (AUDIO signal)



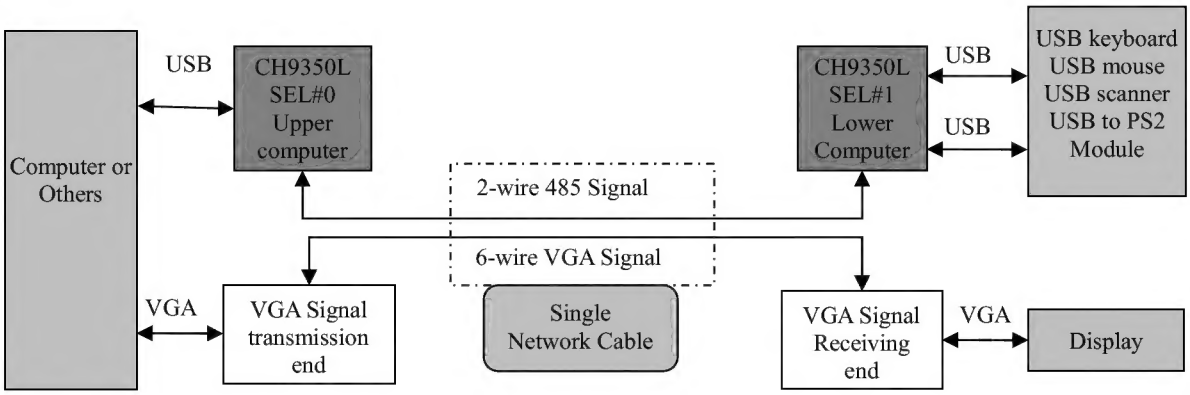
Solution 2: A keyboard, mouse, audio, and video extension solution that integrates USB keyboard and mouse, video signal (DVI signal), and audio signal (AUDIO signal)



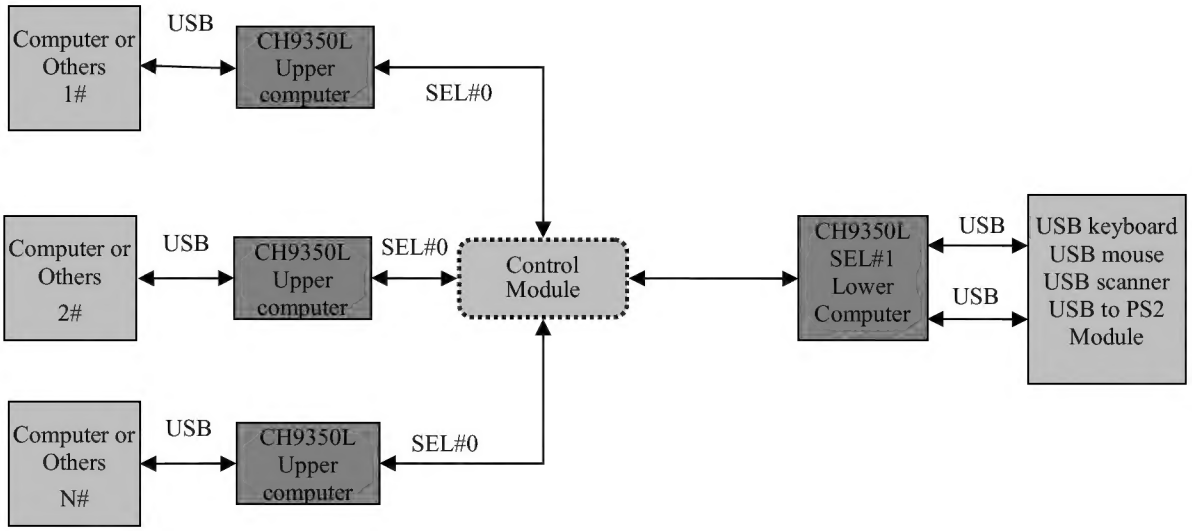
Solution 3: A keyboard, mouse, audio, and video extension solution that integrates USB keyboard and mouse, video signal and audio signal (HDMI signal)



Solution 4: A solution to extend USB keyboard, mouse and video (VGA signal) through a single network cable



Solution 5: KM synchronizer, used for one-to-many, a pair of keyboard and mouse can be used on multiple computers at the same time. After CH9350L enters the upper computer mode, the SEL pin is the UART receiving enable pin, active at low level. By controlling the level state of the SEL pin or switching the UART communication interface, CH9350L module can be specified to work, realizing the KM switching function.


Computer or Others 1#
USB
CH9350L Upper computer
SEL#0
Computer or Others 2#
USB
CH9350L Upper computer
SEL#0
Control Module
CH9350L SEL#1 Lower Computer
USB
USB
USB keyboard USB mouse USB scanner USB to PS2 Module
Computer or Others N#
USB
CH9350L Upper computer
SEL#0